Abstract

It is an object to implement a small-scale data input/output mechanism to a memory at a high speed with a priority all the time for a memory provided in a processor.

[Means for Resolution] In an information processing apparatus including a processor for carrying out a pipeline processing over an instruction, a memory provided in the processor and input/output control means for giving access to the memory with a high priority, a memory access arranging method includes a step (S512) of causing a clock to be supplied to the processor to wait when a contention of access of the processor and the input/output control means to the memory is generated, a step (S506) of executing the access of the input/output control means to the memory, and a step (S507, S511) of canceling the clock wait of the processor after ending the access of the input/output control means to the memory, and executing the access of the processor to the memory.